P4-26: Resilient Systems

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

SHREC Annual Workshop (SAW25-26)

University of Pittsburgh
BYU BRIGHAM YOUNG UNIVERSITY
VIRGINIA TECH
UF UNIVERSITY of FLORIDA

January 13-14, 2026

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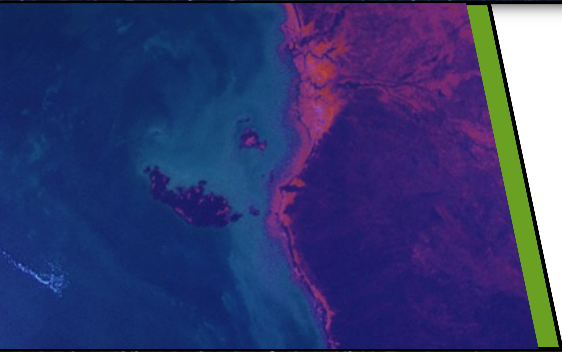
Leo Wylonis [UG]
Graduate Students
University of Pittsburgh

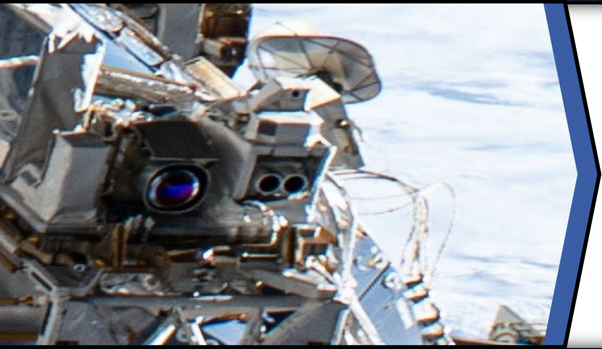
Number of requested memberships ≥ 7

Goals, Motivations, and Challenges



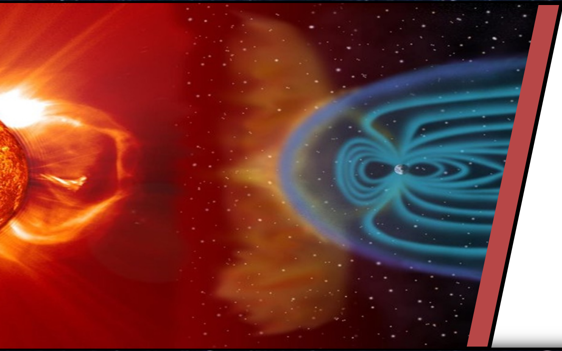
Motivations

- **Advanced sensor technologies** and computational demands **exceed capabilities** that traditional **space-grade processors** can deliver, and gap keeps widening
- **Mission-critical apps** require onboard systems that **reliably** deliver **high performance, energy-efficiency, and affordability**



Goals

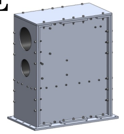
- Explore, prototype, test, evaluate, optimize **new HW and SW modules for space computing**
- **Characterize and improve their ability to operate in harsh environments** of space missions
- Build upon novel SHREC concept of ***hybrid systems*** – novel **mix of Rad-Hard and COTS to achieve Rad-Tolerant** for high reliability and performance with low SWaP-C



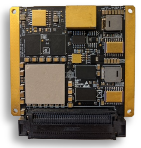
Challenges

- Engineering highly **advanced mission systems** for harsh environments with stringent requirements involves substantial **complexity and expense**
- **New and unproven processors** and system architectures **need extensive evaluation** and verification to guarantee proper **dependability and performance** characteristics

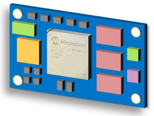
VANTAGE



SSP



SoMs



NVIDIA

GPUs

CPUs

Emulation

Mission-Critical Computing
NSF CENTER FOR SPACE, HIGH-PERFORMANCE, AND RESILIENT COMPUTING (SHREC)

STP-H7 Photo
This payload was integrated and flown under DoD STP - Houston leadership; photo credit NASA

SWaP-C: Size, Weight, Power, and Cost
CSP: CHREC Space Processor
SSP: SHREC Space Processor

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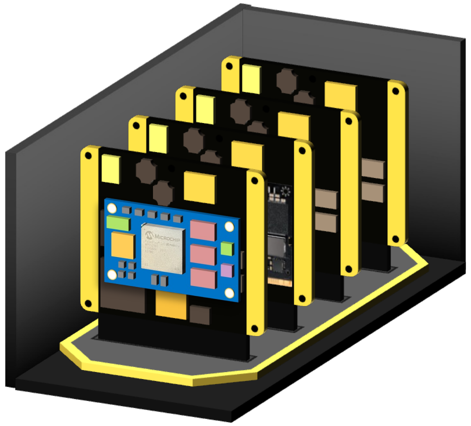
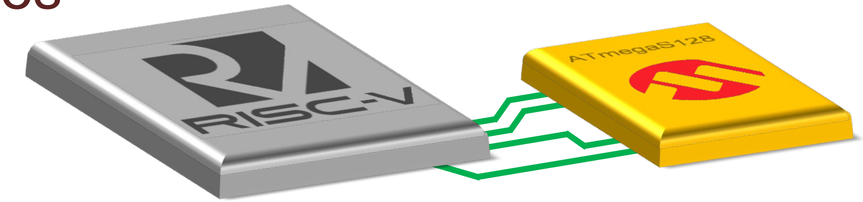
Tasks for 2026

P4



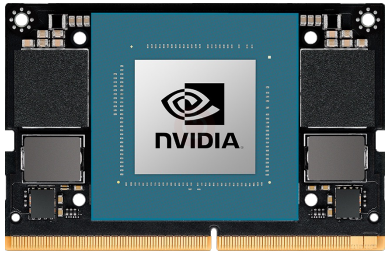
1) Onboard Flight Hardware

- Employ modularity, hybrid electronics, and structural/thermal mech design to develop and test new space technologies



2) Space CPUs

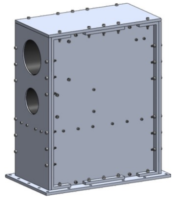
- Research novel approaches with COTS and Rad-Hard devices to combine/balance performance, reliability, and SWaP-C



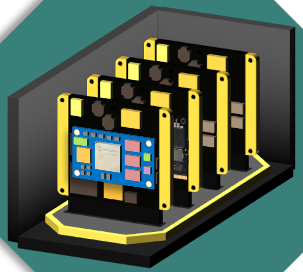
3) Space GPUs

- Investigate, prototype, and evaluate novel hybrid modules and subsystems to exploit massive parallelism of GPUs in space

4) Spacecraft and Mission Emulation



- Explore and advance digital twins and hardware-in-the-loop techniques for onboard payload verification and validation



Task 1
Onboard Flight Hardware

Employ modularity, hybrid electronics, and structural/thermal mechanical design to develop and test new space technologies

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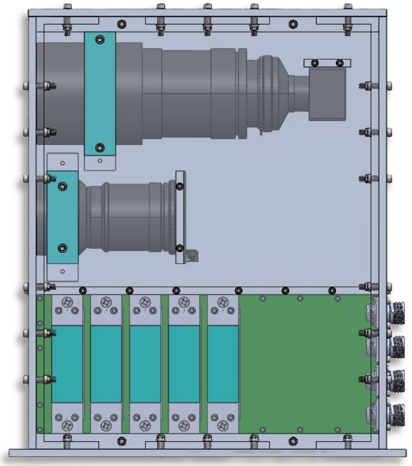
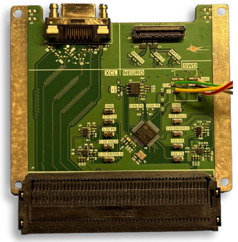
P4

T1: Onboard Flight Hardware





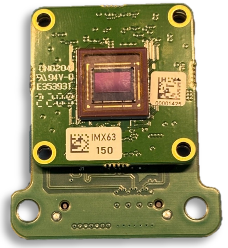
1 Space Avionics

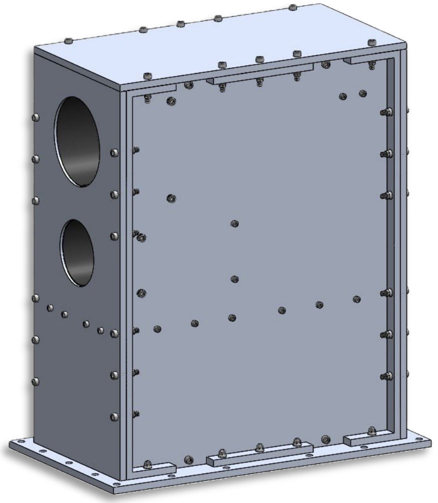
- Achieve **critical VANTAGE milestones** including **CDR and FCA**
- Complete **flight hardware** design, fabrication, and validation
- Perform final VANTAGE flight **avionics integration** and testing

2 High-Throughput Sensing

- Implement custom **FPGA IP** to enable **capture and transmission** of RGB and neuromorphic **sensor data** for VANTAGE
- Research and demonstrate **simultaneous triggering and data acquisition** of onboard sensor data

AMD XILINX



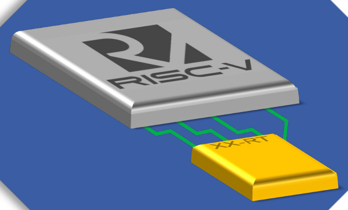


3 Mechanical and Thermal Systems

- Evaluate **structural and thermal** properties of **VANTAGE lenses**
- Conduct verification of **system design in Ansys**
- Complete chassis **fabrication and assembly**

Ansys

CDR:	Critical Design Review
FCA:	Functional Configuration Audit
VANTAGE:	Visual and Neuromorphic Tracking and Geosensing Experiment



Task 2
Space CPUs

Research novel approaches with COTS and Rad-Hard devices to combine and balance performance, reliability, and SWaP-C

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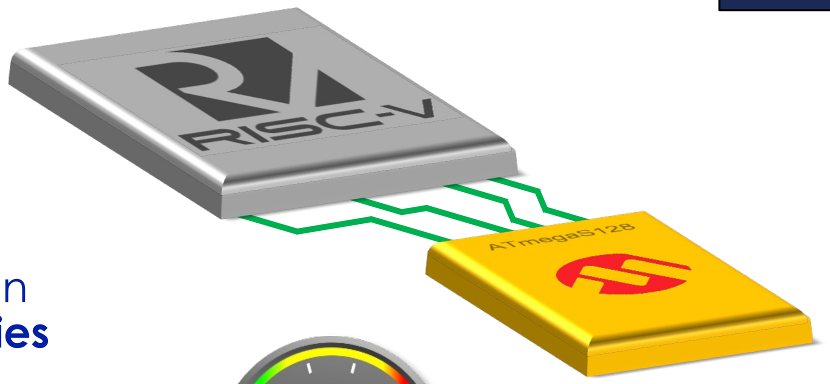
T2: Space CPUs



1 Onboard Fault Characterization and Mitigation

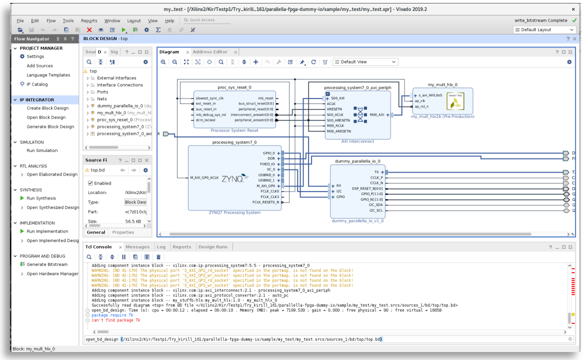
- Exploit **radiation test campaigns** to identify failure modes of next-gen computers (**CPU**, **memory**, **SSD**, etc.) and explore **mitigation strategies**
- Design and test framework for **RT MCU Coprocessor** to **monitor COTS SoCs** for in-flight faults

2 HPSC Resilience and Performance Studies

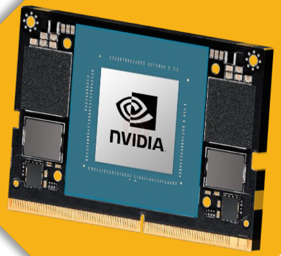
- Conduct comprehensive kernel and app benchmarking studies to **characterize performance and resilience modes of HPSC**
- Study and evaluate various on-chip and interface features to exploit and maximize **HPSC** and other **new RISC-V technologies**

3 Resilient RISC-V Chip Design with Synplify

- Synthesize **processor pipelines** for **radiation test** campaigns using **Synopsys Synplify**
- Develop **Verilog parsers** for **Hamming-3 encoding** within finite state machines in **soft SoCs**



RT: Radiation-Tolerant
MCU: Microcontroller
COTS: Commercial Off-The-Shelf



Task 3
Space GPUs

Investigate, prototype, and evaluate novel hybrid modules and subsystems to exploit massive parallelism of GPUs in space

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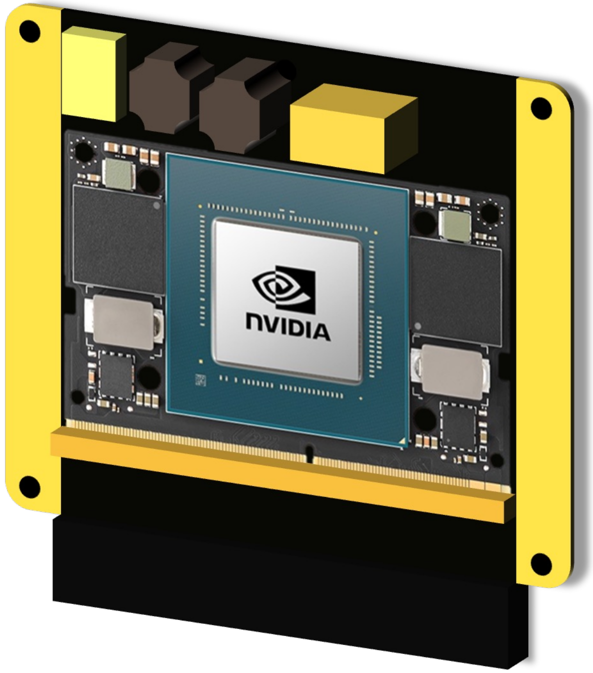
T3: Space GPUs



1

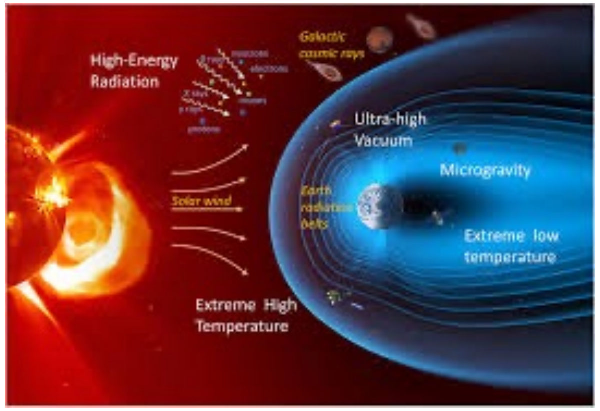
Hybrid GPU SoM Carriers for Control-Error Mitigation

- Fabricate, test, and optimize **new Rad-Tolerant GPU SoM carrier cards**, featuring hybrid mix of Rad-Hard and COTS devices
- Verify efficacy of **mitigation strategies** with **injection and radiation testing**, where our focus is **control errors**

2

Resilient GPU Apps and Toolsets for Data-Error Mitigation

- Conduct assessment of promising **GPU apps and productivity toolsets for space** and identify **reliability limitations and opportunities**
- Investigate and evaluate **new HW, Info, and SW redundancy strategies** for space GPU apps and toolsets, where our focus is **data errors**



3

Space GPU Design Guidelines

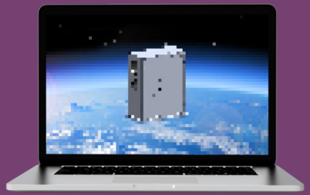
- Leverage **soft-error mitigation** research to create guideline set for **reliable GPU deployment** in various space environments
- Develop **design strategies and trade space** to target more hybrid SoM carrier cards for **broader range of space missions and hazards beyond LEO**

COTS: Commercial off-the-Shelf
SoM: System-on-Module

VANTAGE: Visual and Neuromorphic Tracking and Geosensing Experiment
RTF: Resilient TensorFlow

Task 4

Spacecraft and Mission Emulation



Explore and advance digital twins and hardware-in-the-loop techniques for onboard payload verification and validation

Kushal Parekh

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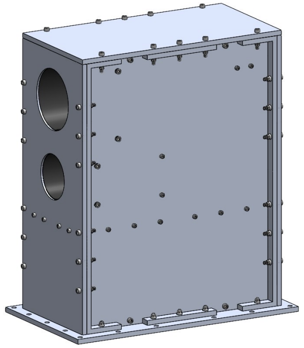
T4: Spacecraft and Mission Emulation

1 Virtualization in NOS3

- Expand **virtual camera features** through GPS-based capture systems and multi-capture functionality
- Enhance C&DH fidelity in for **realistic operations simulations**

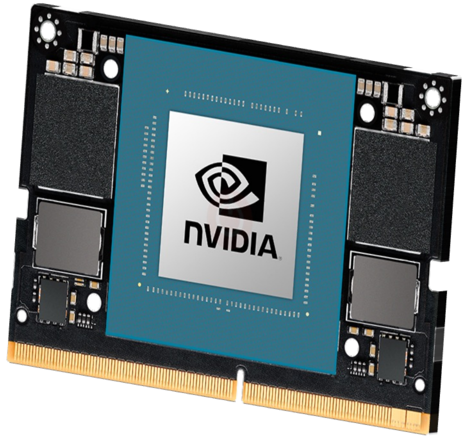


2 QEMU Modeling

- Develop and test **SSP model using QEMU**
- Successfully operate flight-like **OS kernel**
- Incorporate **modular design** for simple use with future missions

3 Space GPU Simulation

- Design host GPU and external GPU interfaces for QEMU and NOS3 applications
- **Compare and analyze simulation vs. real hardware** fidelity and performance metrics



NOS3: NASA Operational Simulator for Small Satellites
VANTAGE: Visual and Neuromorphic Tracking and Geosensing Experiment
C&DH: Commanding and Data Handling
QEMU: Quick Emulator
SSP: SHREC Space Processor

Milestones and Deliverables

- **Milestones**
  - SMW (Summer 2026): Showcase midterm results on all projects
  - SAW (January 2027): Demonstrate completion of all projects

- **Deliverables**
  - Monthly progress reports from all projects
  - Midyear and end-of-year full reports from all projects
  - 3-4 conference/journal papers (~1 per project)
  - Flight carriers for Jetson Orin NX and PolarFire SoC SoMs
- **Budget** (**7+** memberships, or **350+** votes)

Conclusions & Member Benefits

- **T1:** Employ modularity, hybrid electronics, and structural/thermal mech design to **develop and test new space technologies**
- **T2:** Research novel approaches with COTS and Rad-Hard devices to **combine/balance performance, reliability, and SWaP-C**
- **T3:** Investigate, prototype, and evaluate novel hybrid modules and subsystems to **exploit massive parallelism of GPUs in space**
- **T4: Explore and advance digital twins** and hardware-in-the-loop techniques for onboard payload verification and validation

- **Member Benefits**
  - Direct influence over research direction and projects
  - Direct benefit from hardware designs, software applications, and architecture investigations
  - Direct benefit from research study insights